	GESADC-12A
	INTERFACE

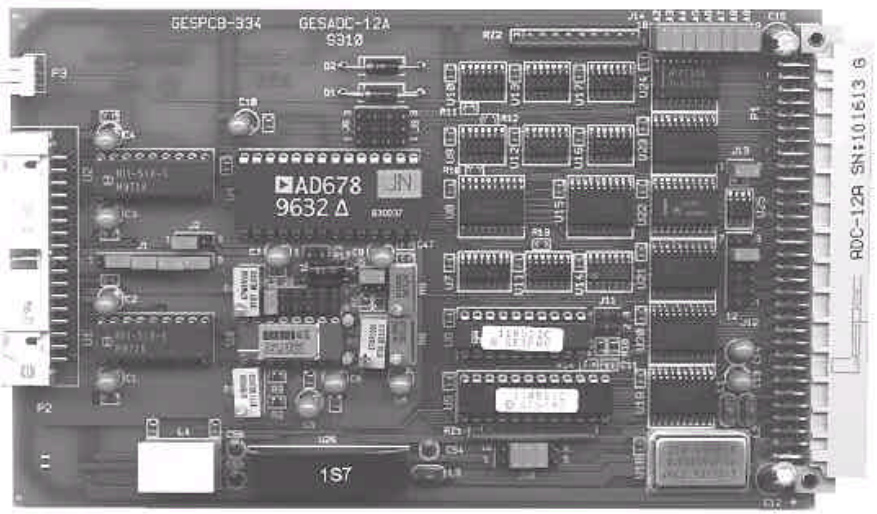
Revision 1.1

FAST 16 CHANNELS, 12-BIT DATA ACQUISITION MODULE

The GESADC-12A module provides the user with a smart and economical solution for analog signal acquisition and conversion into digital information. This board is built around the well known AD1678 analog to digital converter. Analog inputs are possible for 16 single ended channels, or for eight differential channels. Furthermore, an instrumentation amplifier provides additional choices of different selectable gains of 10, 100, 200, or 500. This module is compatible with the G-64/G-96 Bus.

Technical Features

- 16 single ended or 8 differential input channels
- 12-bit resolution ±1/2 LSB
- Analog input range:
- ±5V and ±10V Bipolar (two's complement data format)
- 0-10V Unipolar (straight binary data format)
- Conversion time: 5µs max.
- Fast settling time instrumentation amplifier
- Selectable gain of 1, 10, 100, 200, or 500
- Standard power supply: +5V, ±12V



References

GESADC-12A: Fast 16 channels, 12-bit Analog to Digital Converter.

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REVISION HISTORY

Rev	Date (m/d/y)	By	Modification
1.1	10/24/97	PM	Suppression Gesadc-12 and added the control logic

Updated revision of this document can be obtained on the Gespac Web sites:
http://www.gespac.com (USA site)
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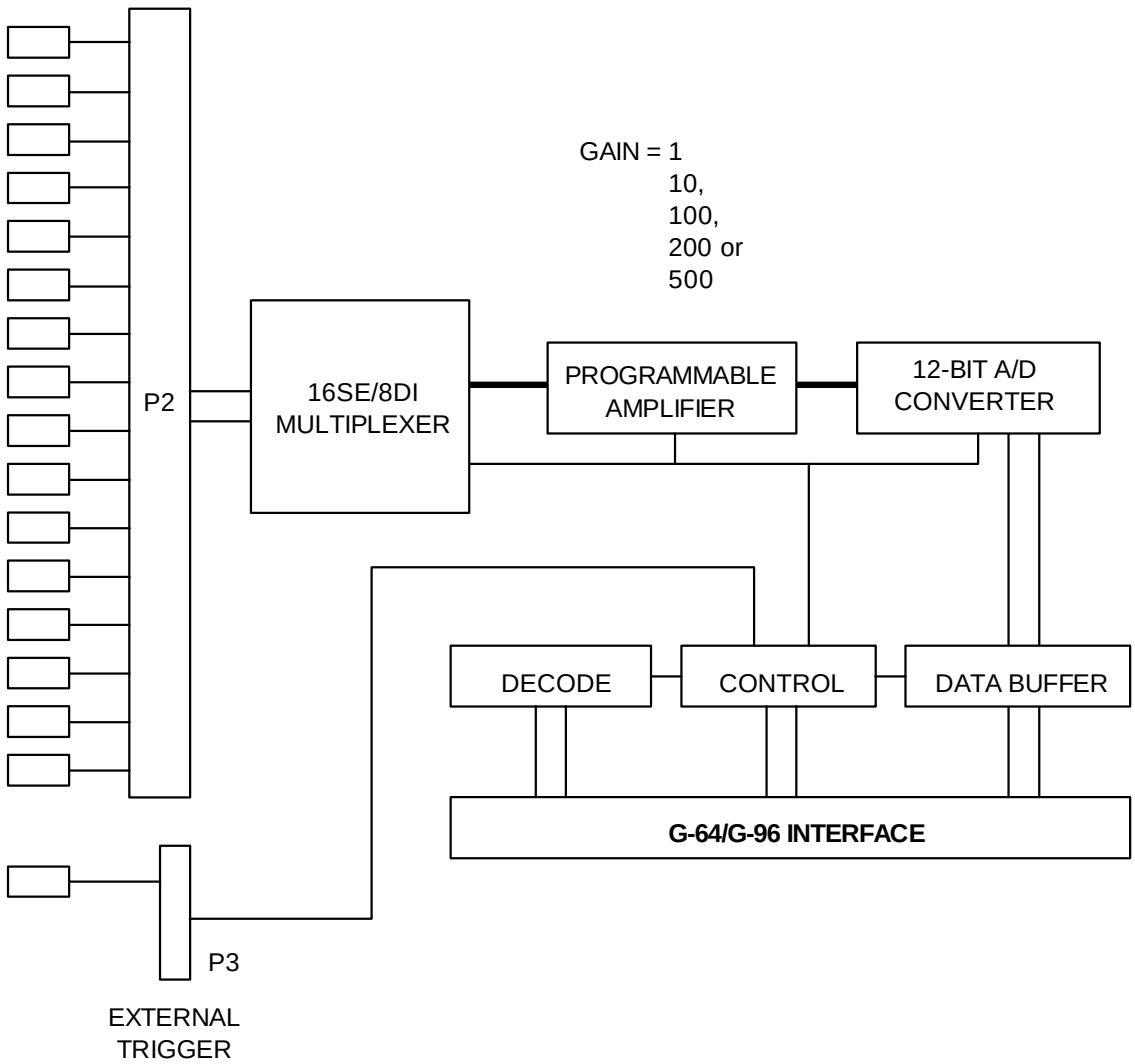


Figure 1.1 Block diagram

1. GENERAL INFORMATION

1.1 DESCRIPTION

The GESADC-12A board is a complete analog acquisition module well suited in industrial applications requiring a large number of analog inputs. The GESADC-12A module can accept up to sixteen analog inputs in the single ended mode or up to eight differential analog inputs. The board includes analog multiplexers, a fast sample and hold device to allow acquisition of fast analog signals, and an instrumentation amplifier with a gain range of 1 to 500.

An A/D conversion can be initiated by a start command written into the control register or by an external trigger signal. When the conversion is complete, either a status bit is asserted for programmed acquisition or an interrupt is generated, if enabled, for interrupt driven acquisition operation. The interrupts generated by the GESADC-12A board can be autovectored or vectored according to the G-64 Bus specifications. The GESADC-12A is built around the AD1678 A/D converter which provides a 12-bit resolution and a linearity error of ±1 LSB.

The GESADC-12A board is compatible with the G-64/G-96 Bus. The block diagram in figure 1.1 illustrates the different module parts and their interconnections.

1.2 SPECIFICATIONS

Analog inputs: Input voltage range:	•16 single ended inputs •8 differential inputs •0V to 10V unipolar mode (Gain =1) •±5V bipolar mode (Gain = 1) •±10V bipolar mode (Gain = 1)
Resolution Input impedance: Acquisition time: Multiplexer selection: Amplifier response: Aperture delay: A/D conversion time: System throughput:	12-bit 10M (single ended) 5µs max. 1.5µs 2.5 MHz (Gain =1) to 100 KHz (Gain = 500) 20ns 4.5µs 200 kilosamples/sec max.
Bus interface: Drivers:	•Address bus: TTL compatible •Data bus: 3-state TTL compatible •48mA devices
Power requirements: Operating temperature: PCB dimensions:	+5Vdc: 120 mA typ. +12Vdc: 50 mA typ. -12Vdc: 50 mA typ. +5 ° C to +55°C 100 x 160 mm

Table 1.1 Specifications

2. PREPARATION FOR USE, INTERCONNECTIONS

2.1 CONNECTOR AND JUMPER IDENTIFICATION

Table 2.1 identifies the jumpers and connectors of the GESADC-12A module. Figure 2.1 shows their locations on the printed circuit board.

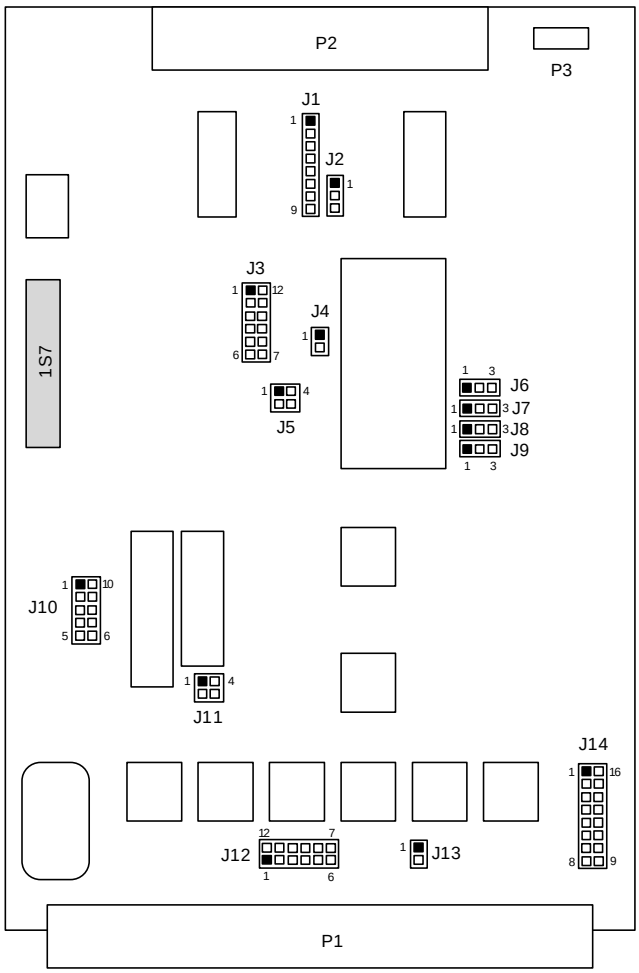


Figure 2.1 Implementation

Designation	Function
P1	G-96 Bus interface connector
P2	Analog input signal connector
P3	Ext. trigger
J1	•Single ended/Differential mode selector •External/Internal analog ground selector
J2	Single ended/Differential mode selector (Multiplexer) Instrumentation amplifier gain selector
J3	± 10V bipolar mode selector
J4	Unipolar/Bipolar operation mode selector
J5	Not used: Factory set
J6-J9	Interrupt acknowledge selection
J10	•Selection synchronous/asynchronous access
J11	•8 or 16-bit bus mode Interrupt line selector
J12	DTACK selection
J13	Module base address selector
J14	Test point: Analog GND
TP1	Test point: Instrumentation amplifier output
TP2	

Table 2.1 Connector, Jumper and Switch Identification

2.2 MODULE ADDRESS SELECTION

The GESADC-12 module can be located anywhere in the VPA field, the J14 jumpers define the module base address according to table 2.2.

J14 POSITION	JUMPER ON	JUMPER OFF
1 ○ 16	A2	A2
2 ○ 15	A3	A3
3 ○ 14	A4	A4
4 ○ 13	A5	A5
5 ○ 12	A6	A6
6 ○ 11	A7	A7
7 ○ 10	A8	A8
8 ○ 9	A9	A9

Table 2.2 Module Address Selection

2.3 INTERRUPTS

2.3.1 INTERRUPT OPERATION MODE SELECTION

The GESADC-12A module can generate an interrupt and also provide an interrupt cycle. The behavior of the GESADC-12A module during an interrupt acknowledgment cycle is controlled by some rules described in table 2.3.

1 One **level**[1] of vectored interrupt (G-64): IF - An interrupt is pending - IACK signal asserted - Chain In signal true THEN - The module provides an interrupt vector
2 **Multilevel**[1] of vectored interrupt (G-64): IF - An interrupt is pending - IACK signal asserted - Chain In signal true - The **priority level**[1] of the module matches the encoded level on A0-A1-A2 bus lines THEN - The module provides an interrupt vector

Table 2.3 Vectored Interrupt Mode Criteria

Note: [1]These parameters are programmable by J10 jumpers

J10 POSITION	JUMPER ON	JUMPER OFF	DESCRIPTION
1 □ ○ 10 2 ○ ○ 9 3 ○ ○ 8 4 ○ ○ 7 5 ○ ○ 6	One	Multi	Operation mode selection
	-	-	Do not care
	$\overline{IPL0}$	IPL0	LSB int. priority level (A0)
	$\overline{IPL1}$	IPL1	(A1)
	$\overline{IPL2}$	IPL2	MSB int. priority level (A2)

Table 2.4 J10 Jumper Description

Note: the vectored mode may be disabled by setting the interrupt priority level of the GESADC-12A to zero. In this case, the module generates an interrupt request but does not provide an interrupt vector. This mode is called autovectored.

IPL2	IPL1	IPL0	PRIORITY	OPERATION MODE
0	0	0	None	Autovectored - no vector
0 0 0 1 1	0 1 1 0 0	1 0 1 0 1	1 2 3 4 5	Vectored-The GESADC-12A module provides an interrupt vector during an interrupt acknowledgment cycle.
1	1	X	-	Reserved - do not use

Table 2.5 Operation Mode Selection

2.3.2 IACK SENSE SELECTION

To ensure the compatibility between the G-64 Bus and the G-96 Bus, the sense of the IACK signal is determined by jumper J10.

J10 POSITION	J10 POSITION
1 □ ○ 10 2 ○ ○ 9 3 ○ ○ 8 4 ○ ○ 7 5 ○ ○ 6	1 □ ○ 10 2 ⊠ 9 3 ○ ○ 8 4 ○ ○ 7 5 ○ ○ 6
IACK signal (G-64)	$\overline{IACK}$ signal (G-96)

Table 2.6 IACK / $\overline{IACK}$ Signal Selection

2.3.3 INTERRUPT OPERATING MODE

The GESADC-12 board must provide a DTACK signal during an interrupt cycle in asynchronous systems. The J13 jumper provides this selection as illustrated in table 2.7.

J13 POSITION	J13 POSITION
1 □ ○ 2	1 ⊠ 2
No $\overline{DTACK}$ signal	With $\overline{DTACK}$ signal

Table 2.7 $\overline{DTACK}$ Signal Selection

2.3.4 INTERRUPT SELECTION

Interrupt requests of the GESADC-12A module are wired on NMI, IRQ1 to IRQ5 bus lines according to J12.

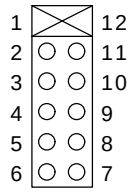
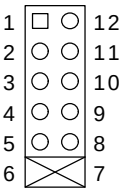
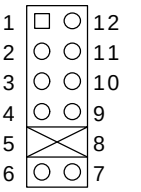
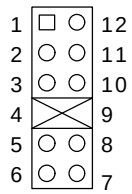
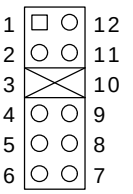
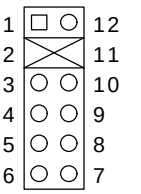
J12	J12	J12
 $\overline{\text{NMI}}$ bus line	 $\overline{\text{IRQ5}}$ bus line	 $\overline{\text{IRQ4}}$ bus line
J12	J12	J12
 $\overline{\text{IRQ3}}$ bus line	 $\overline{\text{IRQ2}}$ bus line	 $\overline{\text{IRQ1}}$ bus line

Table 2.8 Interrupt Line Selection

2.4 ANALOG INPUT SELECTION

2.4.1 SINGLE ENDED/DIFFERENTIAL INPUT SELECTION

The analog inputs of the GESADC-12A module can be used either as sixteen single ended channels or as eight differential channels according to jumper J1.

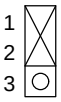
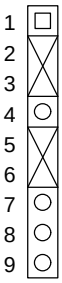
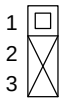
16 SINGLE ENDED CHANNELS		8 DIFFERENTIAL CHANNELS	
J1	J2	J1	J2
			

Table 2.9 Analog to Digital mode Selection

2.4.2 PSEUDO DIFFERENTIAL MODE SELECTION

In the single ended mode, the negative output of the instrumentation amplifier can be connected to the internal analog ground for single ended signal connection, or to an external analog ground used as a sense line for pseudo differential signal connection.

The pseudo differential mode can be used in applications where all inputs have the same ground potential or the ground reference is floating to avoid ground loop current. The pseudo differential mode selection is shown in table 2.10.

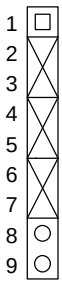
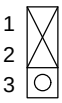
J1	J2
	

Table 2.10 Pseudo Differential Mode Connection

2.4.3 ANALOG INPUT RANGE

The GESADC-12A module works with different input voltage ranges in Bipolar or Unipolar mode. Note that when using the Instrumentation Amplifier, the input voltage ranges given in table 2.11 can be divided by 10, 100, 200, or 500 according to the amplifier gain setting.

Mode	Unipolar	Bipolar	Bipolar
Range	0 to +10V	-5V to +5V	-10V to +10V
J5			
J4			

Table 2.11 Input Voltage Range - Unipolar/Bipolar Mode Selection

2.5 INSTRUMENTATION AMPLIFIER

2.5.1 GAIN ADJUSTMENT

The IN110 instrumentation amplifier provides five fixed gains of 1, 10, 100, 200, and 500 programmable through J3 jumpers.

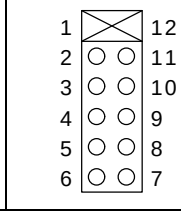
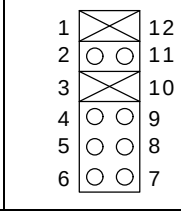
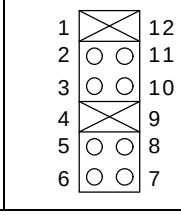
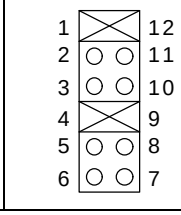
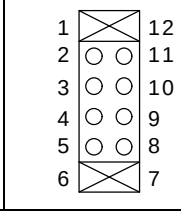
GAIN	1	10	100	200	500
J3					

Table 2.12 Fixed gains

2.5.2 DELAY TIME ADJUSTMENT FOR SETTLING TIME

When the programmable amplifier is used, a delay must be provided between the time the channel is selected and the start of the conversion. The user must provide a delay by software in accordance with table 5.1.

2.6 EXTERNAL TRIGGER

A data acquisition can be initiated by an external trigger signal connected to connector P3. Note that the trigger signal pulse must be active at the low level for a minimum duration of 150ns to be valid. Section 2.7 describes the P3 connector pinout.

PIN	DESIGNATION
1	GND
2	ExTRIG*
3	GND

Table 2.13 P3 Pin Assignment

2.7 ANALOG INPUT CONNECTOR

The analog data acquisitions are made through connector P2. The pin assignment of this connector is given in table 2.14.

PIN	DESIGNATION	SIGNAL DESCRIPTION
31 27 23 19 15 11 7 3	CH0 CH1 CH2 CH3 CH4 CH5 CH6 CH7	Analog inputs
32 28 24 20 16 12 8 4	CH8/RET0 CH9/RET1 CH10/RET2 CH11/RET3 CH12/RET4 CH13/RET5 CH14/RET6 CH15/RET7	Analog inputs or return inputs used together with CH0-CH7
33	Ext. TRIG	Signal when AD conversion must be initialized externally
34	Digital GND	Module digital ground, can be used as return signal for Ext. TRIG
1,5, 913, 172 1,25 29	Ext. GND	Ext GND reference for pseudo differential modes or internal analog GND for other modes
2,6, 10,1 418, 222 6,30	Analog GND	Module analog GND
1. Unused analog inputs should be connected to the analog ground. 2. For low level applications, it is advisable to operate the system as an 8 channel differential input. For best noise rejection, use twisted shielded pair cable.		

Table 2.14 P2 Pin Assignment

2.8 INTERFACE WITH THE G-96 BUS

The GESADC-12A module interconnects directly on a G-96 Bus. Signals used by the module are identified in table 2.15. For more information about the bus timing, refer to the G-64/G-96 Bus Specifications Manual.

ROW C	ROW B	ROW A		Definition
GND	GND	GND	1	Power
A16 *	A8	A0	2	
A17 *	A9	A1	3	
A18 *	A10 *	A2	4	Address
A19 *	A11 *	A3	5	lines
A20 *	A12 *	A4	6	A0 to A23
A21 *	A13 *	A5	7	
A22 *	A14 *	A6	8	
A23 *	A15 *	A7	9	
BWD *	BRQ *	BGRT *	10	
BARB *	DS1	DS0	11	
LWORD *	BBUSY *	HALT *	12	
GND *	ENABLE *	SYCLK *	13	Control &
Reserved *	RES	VPA	14	Interrupt
Reserved *	NMI	RDY/DTACK	15	lines
IRQ3	IRQ1	VMA *	16	
IRQ5	IRQ2	R/W	17	
VED *	IACK	IRQ4	18	
GND	D12	D8	19	
P5 *	D13	D9	20	
P4 *	D14	D10	21	Data lines
P3 *	D15	D11	22	D0 to D15
P2 *	D4	D0	23	&
P1 *	D5	D1	24	Arbitration
P0 *	D6	D2	25	lines
Reserved	D7	D3	26	
SYSFAIL *	BERR *	PAGE *	27	Miscel-
Reserved	CHAIN IN	CHAIN OUT	28	laneous
Reserved	+ 5 V batt.*	PWF *	29	
Reserved	-12 V	+ 12 V	30	Power
+ 5 V	+ 5 V	+ 5 V	31	
GND	GND	AGND	32	

Table 2.15 P1 Connector, G-96 Bus

* Not used by the GESADC-12A module.

2.9 BUS ACCESS MODE SELECTION

The GESADC-12A can be configured to work with 8- or 16-bit processors, synchronous or asynchronous. In 8-bit mode, two successive accesses to the data register are needed to acquire the result of the conversion. The data is left justified.

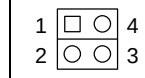
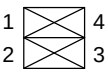
J11	J11	J11	J11
			
16-BIT MODE ASYNC	8-BIT MODE ASYNC	16-BIT MODE SYNC	8-BIT MODE SYNC

Table 2.16 GESADC-12A configurations

3. REGISTER DESCRIPTION

This section contains a brief description of the GESADC-12A registers and the bit assignments within each register. The register location is given in table 3.1.

Upper Byte DATA REGISTER Lower Byte
CONTROL/STATUS REGISTER
INTERRUPT VECTOR REGISTER

Table 3.1 Register Map

3.1 AD1678A - DATA REGISTER

Once it is established that the conversion is finished, the data can be read. The upper data register contains the eight MSBs (DB11-DB4) and the lower data register contains the four LSBs (DB3-DB0) in the upper half of the byte, followed by four trailing zeroes.

Base address + $00:

7	6	5	4	3	2	1	0
DB11 (MSB)	DB10	DB9	DB8	DB7	DB6	DB5	DB4

Base address + $01:

7	6	5	4	3	2	1	0
DB3	DB2	DB1	DB0 (LSB)	0	0	0	0

Figure 3.1 AD1678A - Data Register

3.2 CONTROL REGISTER

The control register is a write-only register. This register controls the different parts of the GESADC-12A module such as the analog input multiplexer, the interrupt logic, the external trigger signal, and finally to start an acquisition. All the control register bits are cleared after a reset operation. The bit assignments are shown in figure 3.2.

Base address + $02 (Write only):

7	6	5	4	3	2	1	0
CONV	IEN	XTRIG	-	CH3	CH2	CH1	CH0

CONV Start Conversion. When this bit is written to a one, the GESADC-12A starts an analog to digital conversion on 12-bits. Writing a zero in this bit location has no effect.

IEN Interrupt Enable. When this bit is a one, the GESADC-12A can generate an interrupt each time a conversion is complete.

XTRIG External Trigger Enable. If this bit is a one, an A/D conversion is processed each time the External Trigger input is driven low. Note that a minimum pulse duration of 150ns is required to ensure operation of the external trigger signal. When the XTRIG bit is a zero, the External Trigger input from P3 is inactive.

CH3-CH0 Channel Selection. These bits select the appropriate analog input channel for conversion. In single ended mode, bits CH3 through CH0 allow selection from one of the 16 channels. In the differential mode, only bits CH2 through CH0 are used to select from one of the 8 differential channels.

Figure 3.2 Control Register Bit Assignment

3.3 STATUS REGISTER

The status register is read-only and provides information on the state of the GESADC-12 module.

Base address + $02 (Read only):

7	6	5	4	3	2	1	0
INT/BSY	IEN	XTRIG	-	CH3	CH2	CH1	CH0

INT/BSY Interrupt Pending/Busy. The meaning of this bit depends on the operating mode chosen to interface with the GESADC-12 module. There are two possibilities:

Programmed Interface (polling mode)

This bit is internally set to a one when a conversion is started by writing a one into the CONV bit location, or by the trigger signal. Once the conversion is complete, this bit is cleared (set to zero).

Interrupt Driven Interface

When the conversion is complete, an interrupt request is generated and the INT/BUSY bit is set to a one, to signal that an interrupt is pending. This bit is cleared by reading the conversion result from the data register.

Note that this selection is made automatically depending on bit IEN.

IEN=0 Polling mode
(BUSY-Bit)

IEN-1 Interrupt driven mode
(INT-Bit)

IEN This bit is the actual state of the IEN-bit in the control register.

XTRIG This bit is the actual state of the XTRIG-bit in the control register.

CH3-CH0 These bits are the value programmed into the control register.

Figure 3.3 Status Register Bit Assignment

3.4 INTERRUPT VECTOR REGISTER

This 8-bit register is used by the GESADC-12A module during interrupt acknowledgment bus cycles and its contents are placed on D0-D7 bus lines. This register is not affected by a reset operation.

Base address + $03:

7	6	5	4	3	2	1	0
IV7	IV6	IV5	IV4	IV3	IV2	IV1	IV0

Figure 3.4 Interrupt Vector Register

3.5 DATA FORMAT

Data is left justified. In these examples, the base address of the board is $800000.

- 8-bit mode

D07-D00								
Base +0 $800001	MSB D11	D10	D09	D08	D07	D06	D05	D04

D07-D00								
Base +1 $800003	D03	D02	D01	LSB D0	X	X	X	X

D07-D00	
$800005	Control/Status

D07-D00	
$800007	Interrupt Vector Register

- 16-bit mode

D15-D08								
$800000	MSB D11							D04

D07-D00								
$800001				LSB D0	X	X	X	X

$800002 Same as $800000

D15-D08								
$800004	X	X	X	X	X	X	X	X

D07-D00	
$800005	Control/Status

D15-D08								
$800006	X	X	X	X	X	X	X	X

D07-D00	
$800007	Interrupt Vector Register

The result of the conversion is:

- Straight binary data format in unipolar mode.
- Two’s complement binary data format in bipolar mode.

UNIPOLAR CODING (Straight Binary)		BIPOLAR CODING (Two’s Complement)	
VIN	OUTPUT CODE	VIN	OUTPUT CODE
0 5.000V 9.9964V	000…0 100…0 111…1	-5.000V -0.002V 0 +2.500V +4.9964V	100…0 111…1 000…0 010…0 011…1

Table 3.1 12-Bit Mode Coding Format (1 LSB=2.44mV)

4. CALIBRATION PROCEDURE

4.1 INSTRUMENT AMPLIFIER

- Connect channel 1 to ground (pins 31 and 30).
- Input offset
  Set a gain of 500.
  Connect a volt meter at the test point TP2.
  Adjust the potentiometer R1 to null the offset.
- Output offset
  Set a gain of 1.
  Adjust the potentiometer R4 to null the offset.

4.2 A/D CONVERTER

- Unipolar mode

  Zero
  Connect channel 1 to ground (P2-pins 31 and 30).
  Start a conversion; read the result.
  Adjust R5 to null the offset.

  Gain
  Apply a +10V signal to channel 1.
  Adjust R8 to have full scale reading from conversion.

- Bipolar mode

  Zero
  To trim bipolar zero to its nominal value, apply a signal 1/2 LSB below midrange (-1.22mV for a ±5V range) and adjust R9 until the major carry transition is located (1111 1111 1111 to 0000 0000 0000).

  Gain
  To trim the gain, apply a signal 1 1/2 LSB below the full scale (+4.9963V for a ±5V range) and adjust R8 to give the last positive transition (0111 1111 1110 to 0111 1111 1111). These items are interactive so several interactions may be necessary for convergence.

5. ADDITIONAL INFORMATION

5.1 INA110 TYPICAL PERFORMANCE

PARAMETER	FIXED GAIN 10	100	500	UNITS
Bandwidth	2	.400	.10	MHz
Slew Rate	12	12	5	V/us
Settling Time 0.01% of 20V	3	7	16	us
Offset Voltage Warm-up Drift	±5	±4	±3	uV
Gain Non-linearity	0.002	0.004	0.01	% of FS
Gain Error	0.01	0.04	0.1	%

Table 5.1 INA110 Instrumentation Amplifier Typical Performance

5.2 PROGRAM EXAMPLE

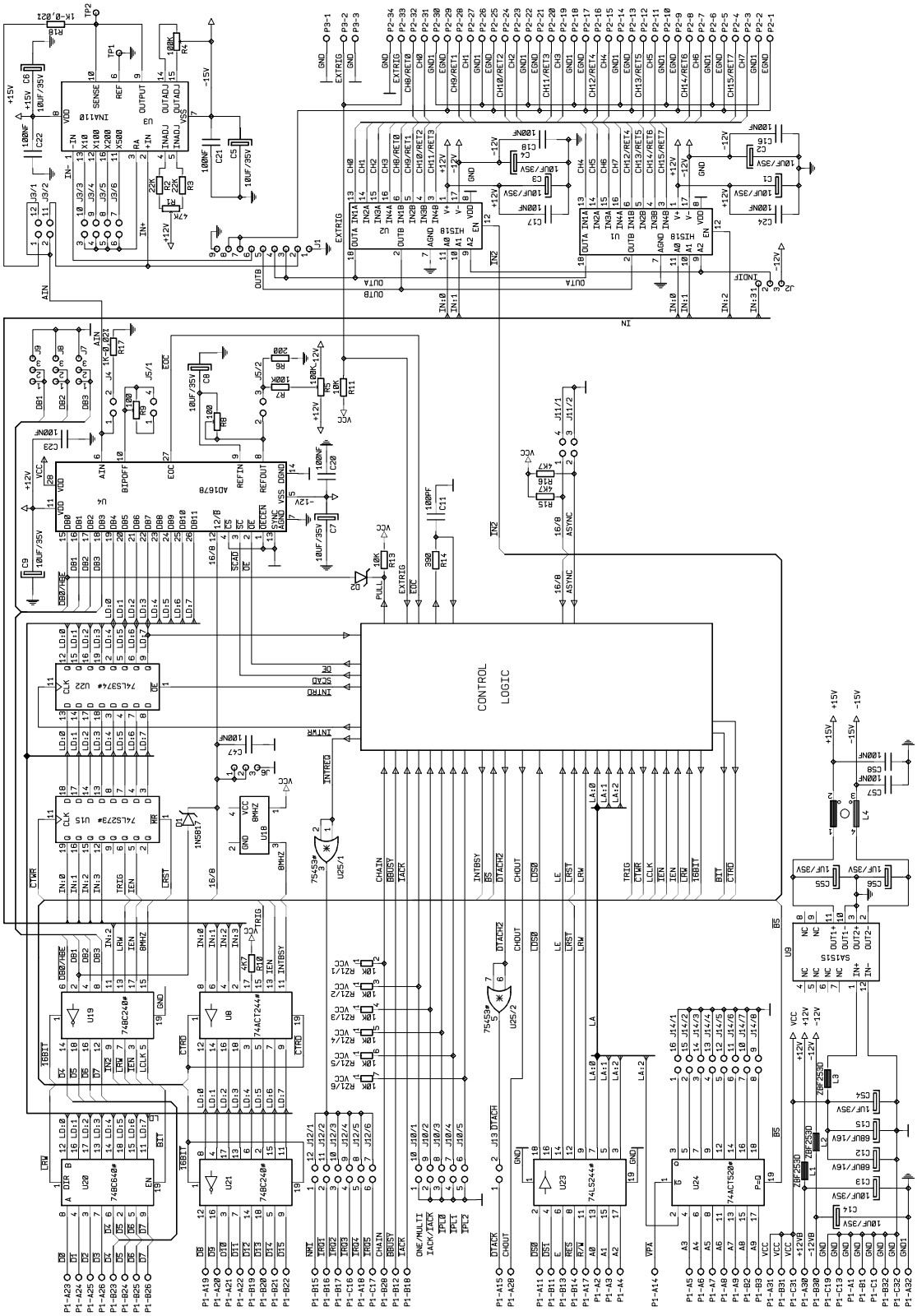
This program uses a GESMPU-4B CPU board, GESDAC-1 board, and a GESADC-12A. It generates a ramp at the output of the first D/A, starts an A/D conversion, and sends the result to the second D/A converter.

```
            LEA.L       $8000100, A0        base address D/A board.
START3      MOVE.W      #$0, D0
START2      MOVEP.W     D0, (A0)            send D0 to D/A.
            LEA.L       $820000, A1         base address A/D board
                                            8-bit mode, asynchronous.
            MOVE.B      #$ 80, 5(A1)        start A/D conversion
WAIT        BTST        #7, 5(A1)           Is conversion finished?
            BNE WAIT
            MOVEP.W     1(A1),D1            Result in D1, left justified
            ROR.W       #4,D1
            MOVEP.W     D1,4(A0)            Send result to second D/A
            ADDI.W      #1,D0
            CMP.W       #$ 1000,D0
            BNE.S       START2
            BRA.S       START3
```

Note: When changing channels a write must be performed of the control register to select the new channel change followed by another write of the control register to start the conversion. This kind of operation guarantees that the input stage has settled before starting conversion.

Select channel 4
move.b #$4,<Control register address>

Start A/D conversion on channel 4
move.b #$84,<Control register address>


CONTROL
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